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Linear CCD shift registers were fabricated in the InGaAs/InAlAs/InP material system as a first step towards developing 1-3 um imaging CCDs. The devices were 38 pixels long with In.53Ga.47As channels. In this Phase I effort, the material was successfully grown and characterized. A process flaw prevented actual clocking of the CCDs. Material and FET characterizations have highlighted issues needing to be resolved during the Phase II program.

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"An Indium Gallium Arsenide Charge-Coupled Device (CCD) for 1-3 μm Imaging"

Contract #DAAL03-92-C-0039

U.S. Army Research Office (Research Triangle, NC)
Dr. Robert Trew (Technical Monitor)

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SBIR Phase I Final Report
May 28, 1993

1. Project Summary

This program was the third in a package of three Phase I programs all designed to advance InGaAs materials technology so that high performance imaging can be performed at room temperature in the 1-3 μm near infrared band. The Programs investigated three different approaches to the problem.

In the first, "A High Performance Room-Temperature Near-Infrared Camera" (SDIO-92/DAAL03-92-C-0040), the emphasis was on a hybrid structure in which an InGaAs two dimensional photodiode array was integrated with a silicon CMOS readout multiplexer using indium bump-bonding techniques. In the second, "A Monolithic InGaAs FET/Detector Array for Near-Infrared Imaging" (NAS7-1181), a first step was taken in the integration of InGaAs planar photodiodes with an InGaAs JFET readout structure.

The present program was the most ambitious and had as its primary objective the fabrication of an InGaAs resistive gate CCD with a long term goal of developing 1-3 μm InGaAs two dimensional imaging CCDs.

The 1-3 μm band, at present, is ill-served for imaging. The existence of a room temperature imager sensitive to this wavelength range is important for a wide variety of defense, scientific, and commercial applications. Operability at room temperature will allow the camera to be miniaturized, reduce its cost, and increase its ruggedness making it well suited for field applications. As a moderate-sensitivity thermal imager, cameras in this range will be able to detect on-coming vehicles and missiles as well as monitor manufacturing processes. This wavelength band also provides a better match to the natural illumination spectrum of the night sky providing enhance Night Vision capability. When combined with long wavelength (ca. 1.55 μm) illumination, covert, eye-safe surveillance is possible. Finally, one and two dimensional InGaAs arrays will span the gap between silicon based focal plane arrays and CCDs and middle infrared imagers and Fourier spectrometers for near infrared spectroscopic applications.

During this Phase I Program, $In_{.53}Ga_{.47}As$ linear CCDs and test structures were fabricated and tested. We were not able to successfully clock entire devices but much useful information on the device and materials structure was obtained. From this and the other two related programs, we conclude that:

1. In the near term, the hybrid approach has the greatest chance of success with state-of-the-art room temperature imaging achieved in the 1-1.7 μm band. To extend this result to 1-3 μm will require substantial advances in both materials and processing technology.

2. As a follow-on technology, the monolithic focal plane array approach is realistic. A Phase II program is currently underway with a goal of demonstrating two dimensional imaging in the 1-1.7 μm band.

3. In the foreseeable future, CCDs are not a viable approach to NIR imaging in the InGaAs system. The reasons for this conclusion are discussed in this report. We do conclude, that the performance of linear CCDs is an excellent way to quantify advances in both materials and process technology.

Based on the above conclusions, a Phase II proposal will be submitted with a goal of using CCDs as a key element in a materials and process development program leading to monolithic, room temperature 1-3 μm imaging.

2. Phase I Technical Objectives

The primary objective of Phase I was to fabricate a CCD in the $In_{.53}Ga_{.47}As/InP$ material system that would detect light between 1.0 and 1.7 μm. This was to lead to a Phase II program that would apply the results to the $In_{.8}Ga_{.2}As/InP$ material system so as to allow detection out to 3.0 μm. In order to develop the Phase I CCD, several device structures were to be characterized for leakage current and FET performance. The specific Technical Objectives were:

1. Obtain $In_{.53}Ga_{.47}As/InP$ wafers with appropriate device structure.

2. Obtain mask set to allow fabrication of test structures, capacitive gate CCDs and resistive gate CCDs.

3. Fabricate test structures and CCDs.

4. Characterize test structures and CCDs.

5. Deliver prototype CCD, Final Report, and Phase II proposal.

3. Work Carried Out/Results Obtained

3.1 Obtain $In_{.53}Ga_{.47}As$/InP wafers with appropriate device structure

In a conventional InGaAs planar photodiode, an unintentionally doped n-type InGaAs active layer is grown on an n^+-InP substrate and the p-n junction is formed by zinc diffusion. In the actual structure (Figure 1), InP layers are grown between the substrate and the active layer to buffer the active layer from defects in the substrate and on top of the active layer to serve as a passivant.

For longer wavelength, lattice mismatched InGaAs photodiodes, the single InP buffer layer is replaced by a stack of thin layers of $In_xGa_{1-x}As$ where x in the individual layers are graded from InP at the substrate to the indium content of the active layer. This "graded" structure accommodates the lattice mismatch between the substrate and the active layer. The cap layer uses an alloy with composition intermediate between the InP substrate and the InGaAs active layer.

A photodiode is a minority carrier device. Photo-generated holes in the n-type region and electrons in the p-type region are swept across the junction where they contribute to the photocurrent.

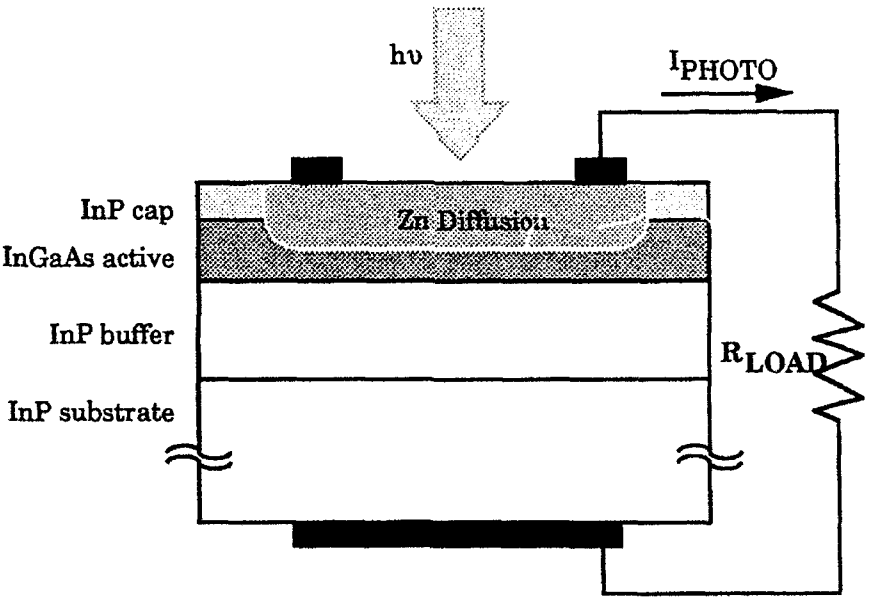


Figure 1: Structure of conventional InGaAs photodiode

CCDs are fundamentally majority carrier devices. Majority carriers are injected into the depleted channel and then clocked to the output node. In III-V materials, the CCD and associated transistors are formed with Schottky barrier gates.

In a capacitive gate CCD, closely spaced electrodes are used to clock charge along the channel. The presence of gaps between gate electrodes introduces potential barriers or troughs under the gap regions with the effects of reduced charge transfer efficiency and dynamic range. The effects of the potential trough can be minimized by reducing the gap size to sub-micron dimensions which greatly increases fabrication difficulty.

An alternative approach is to use a resistive gate structure (Figure 2) in which the entire CCD channel is covered with a resistive material, typically a ceramic/metal alloy (cermet). In this structure, narrow, widely spaced electrodes are used to apply the clock voltages. In addition to simplifying the fabrication and eliminating gap related problems, the use of cermet results in lower leakage contacts than most metals. In this Program, resistive gate CCDs were fabricated.

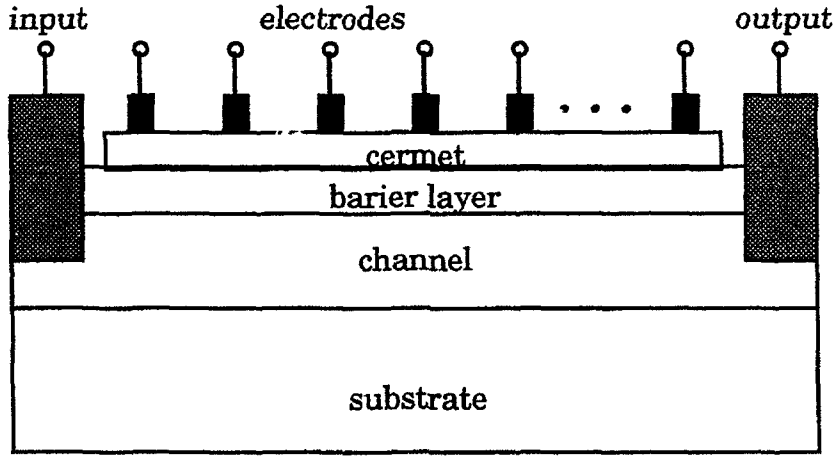


Figure 2: Structure of resistive gate CCD

The objective of this Phase I program was to fabricate an $In_{.53}Ga_{.47}As$ CCD and to observe charge transfer. The specific structure is shown in Figure 3 and was grown by QED (Bethlehem, PA) using molecular beam epitaxy (MBE). Figure 4 is the Growth Verification Form from QED.

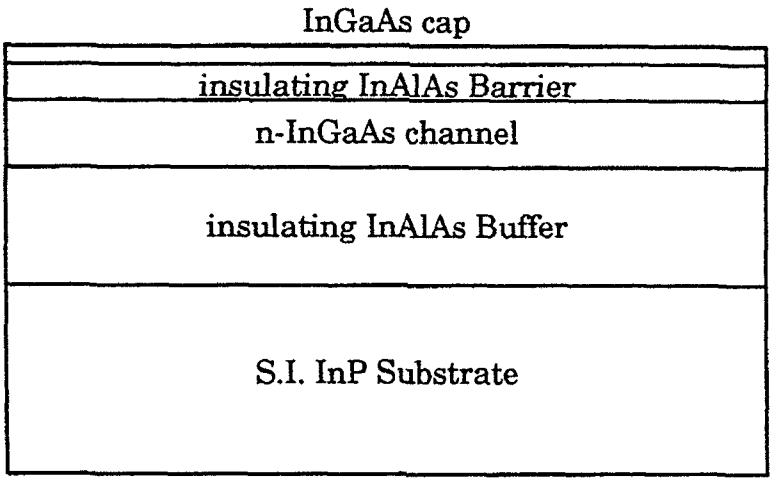


Figure 3: Material structure for InGaAs resistive gate CCD

The channel was a 1500 Å layer of n-type $In_{.53}Ga_{.47}As$ doped to $1x10^{17}$ cm^3. The CCD operates by pinching off the channel against the insulating substrate. While the lattice of $In_{.53}Ga_{.47}As$ is matched to that of the InP substrate, epitaxial material tends to be of better crystal quality than bulk substrate and the use of a buffer layer isolates the channel from defects in the substrate. In a "conventional" photodiode structure grown by vapor phase epitaxy (Figure 1), the buffer is InP. As MBE has difficulty with phosphorous-containing compounds, in this case the buffer was 2500 Å of undoped $In_{.52}Al_{.48}As$ which is also lattice matched to both InP and $In_{.53}Ga_{.47}As$.

A thin (600 Å) layer of undoped $In_{.52}Al_{.48}As$ was also grown on top of the $In_{.53}Ga_{.47}As$ channel. With its higher (than $In_{.53}Ga_{.47}As$) energy bandgap, it increases the effective height of the Schottky barriers without effecting the properties of the channel. This combination of channel and barrier layer properties tends to lead to good breakdown characteristics compared to either thicker channel layers or heavier doping while targeting a pinchoff voltage of about 3 V. The thin cap layer serves to passivate the InAlAs surface and plays no active role in the device.

Growth Verification Form

Customer:	Dr. Greg Olsen	P.O.#	0011
	Sensors Unlimited, Inc.		
	3490 U.S. Route 1		
	Princeton, NJ 08540		
		Date :	October 23, 1992

EPITAXIAL WAFER SPECIFICATIONS

PROFILE	MOLE %	THICKNESS Å	DOPANT	|Nd-Na|
i InGaAs Cap	53	100	None	--------
i InAlAs Barrier	52	600	None	--------
N InGaAs Channel	53	1,500	Si	1.0x1017
i InAlAs Buffer	52	2,500	None	--------
S.I. InP Substrate		350 +/-25μm	Fe	--------

SUBSTRATE SPECIFICATIONS

Material Type:	InP Single Crystal Wafer (LEC)
Dopant:	Fe
Diameter :	50.0+/-0.6 mm
Thickness:	350+/-25um
Flat Orientation:	European- Japanese
Surface Finish	Polished\Etched
Vendor:	
Boule#:	

REQUIRED CHARACTERIZATION

Method:	Yes	No	Specification (± 10% of specification)
Defect Density			

Quantity: 1 Wafer	**Delivery: 5 Weeks**

Approved: Greg Olsen **Date:** 10/27/92

3.2 Obtain mask set to allow fabrication of test structures, capacitive gate CCDs and resistive gate CCDs

The mask set used was based on one developed by the research group of Professor Eric Fossum of Columbia University (now with Jet Propulsion Laboratories). The original mask set contained cells with 14 different CCD structures as well as a cell containing alignment marks and test structures. For this program, we simplified the mask set to contain 3 variations of resistive gate CCDs as well as the test structures. Figure 5 is a drawing of the superimposed mask layout for one of the CCD structures (on this scale, the differences are not discernible). The mask set was purchased from Align-Rite Corporation (Burbank, CA).

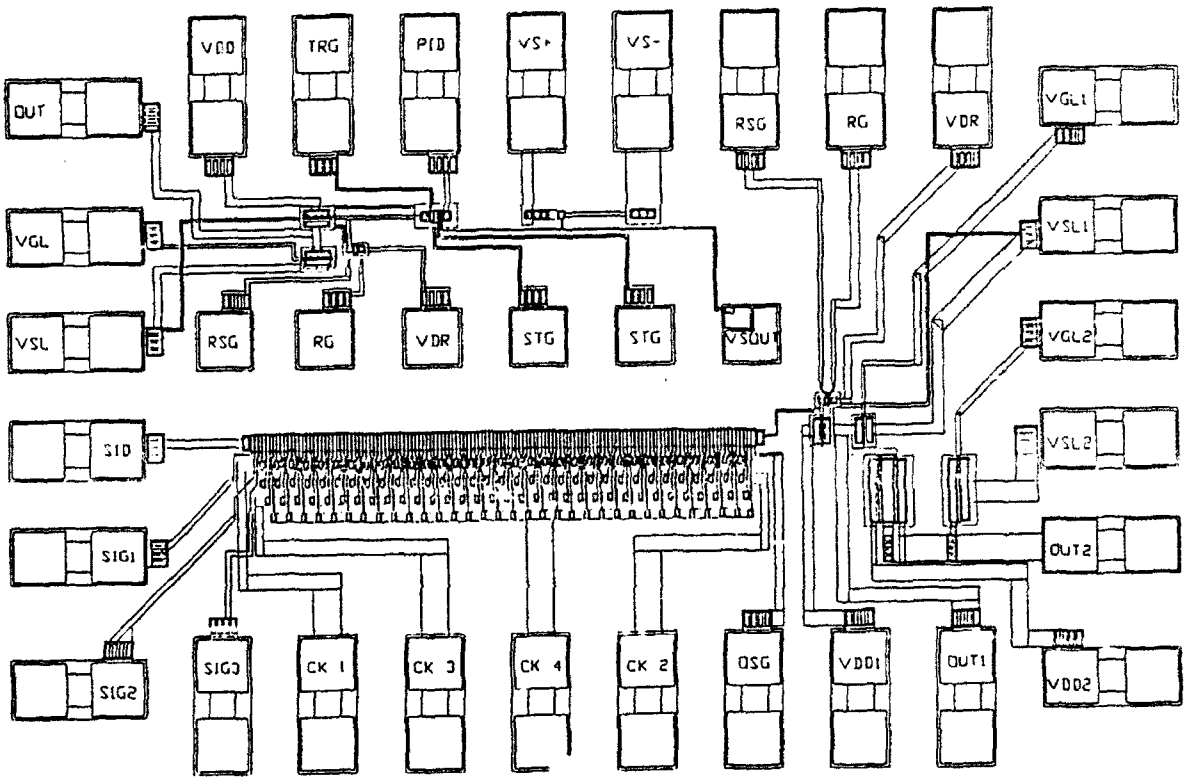


Figure 5: Mask layout of resistive gate CCD

3.3 Fabricate test structures and CCDs

Before photolithography, the wafers were cleaned in a tetrachloroethylene bath at 60 °C using ultrasonic agitation for 7 minutes. This was followed by sequential rinses in acetone (5 minutes), deionized water (1 minute), and methanol (5 minutes). The wafers were dried using high purity N_2.

The first photolithographic step was to isolate the CCD and FET channels using a mesa etch (Figure 6). Photoresist was applied and baked; the mesa mask aligned and exposed; and the photoresist developed. The mesas were etched using a 1:1:38 solution of H_3PO_4:H_2O_2:H_2O) then rinsed under deionized water. Following the etch, the photoresist was stripped in an acetone bath then rinsed and dried.

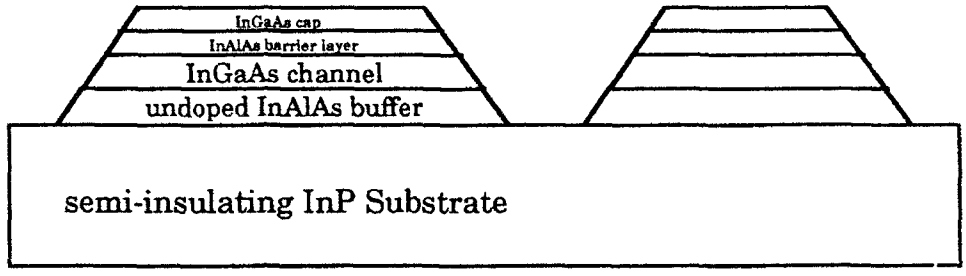


Figure 6: Mesa isolation

After mesa isolation, the ohmic contacts were applied (Figure 7). Following photolithography, 2000 Å of AuGe were evaporated with lift-off in an acetone bath. The contacts were annealed into the wafer at 400 °C for 15 seconds in a rapid thermal annealer.

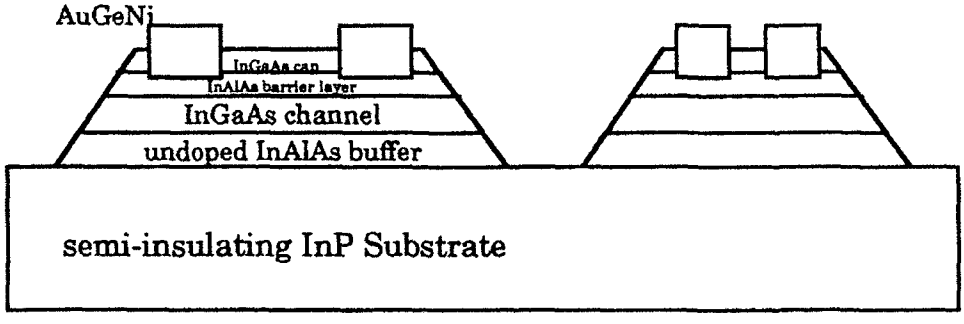


Figure 7: Ohmic contact formation

After the ohmic contacts are formed, the cap layer must be removed prior to the cermet deposition. Recessing the InGaAs cap layer into the InAlAs barrier layer also affects the saturation current and, hence, the pinchoff voltage. During CCD processing, recess etching was performed slowly using a 3:1:300 solution of H_3PO_4:H_2O_2:H_2O. The saturation current measured after each etching period until the target current was attained.

Formation of the resistive gates was performed by lift-off of an electron-beam evaporated equal weight of Cr and SiO powder sources (Figure 8). The mixture and thickness (ca. 1500 Å) was chosen to obtain a sheet resistivity of about 300 kΩ/square.

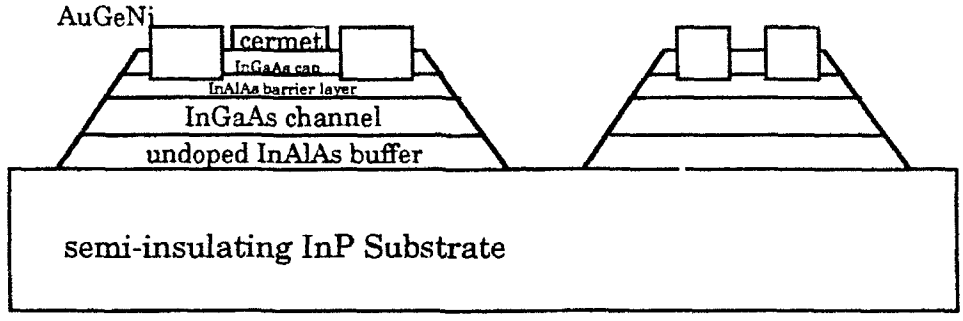


Figure 8: Cermet deposition

Gate electrodes for both the CCDs and the FETs were defined by liftoff of Cr/Au. The Cr was electron-beam evaporated from a mesh/chunk source to a nominal thickness of 50 Å and is used to ensure adhesion of the subsequent 1000 Å thick Au layer.

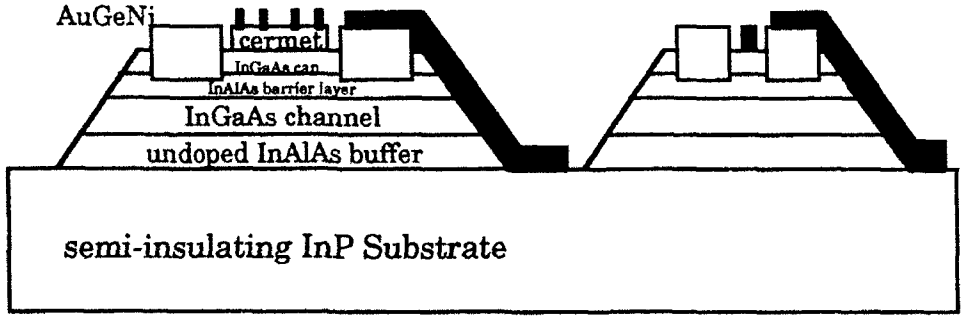


figure 9

Figure 9: Gate metal deposition

Connecting the common phase gate electrodes necessitates the use of a double metal process with the second metal acting as the interconnect. Isolation of the two metals requires a good insulating layer with a low dielectric constant for low parasitic cross-over capacitance. For this purpose about 3000 Å of electron-beam evaporated SiO was used. Vias were formed by lifting off the evaporated SiO (Figure 10).

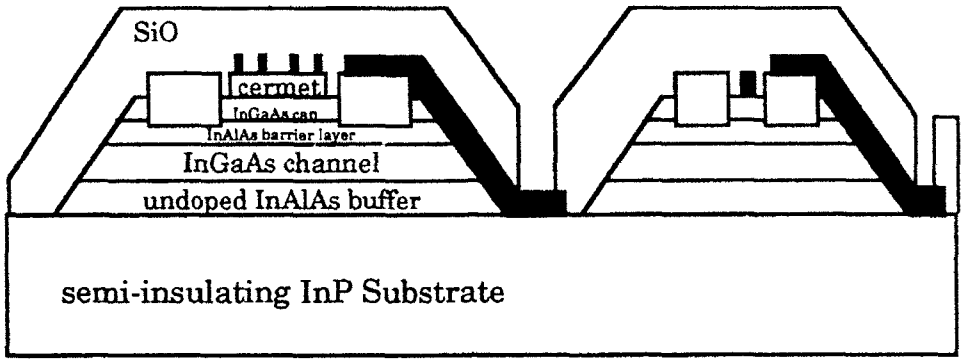


Figure 10: Inter-metal dielectric deposition

The final metallization which serves as the interconnect metal was also Cr/Au. In this case, while the Cr adhesion layer was again about 50 Å thick, the Au layer was typically 5000 Å thick in order to ensure step coverage of the via contact (Figure 11). This metallization also forms the bonding pads for the device.

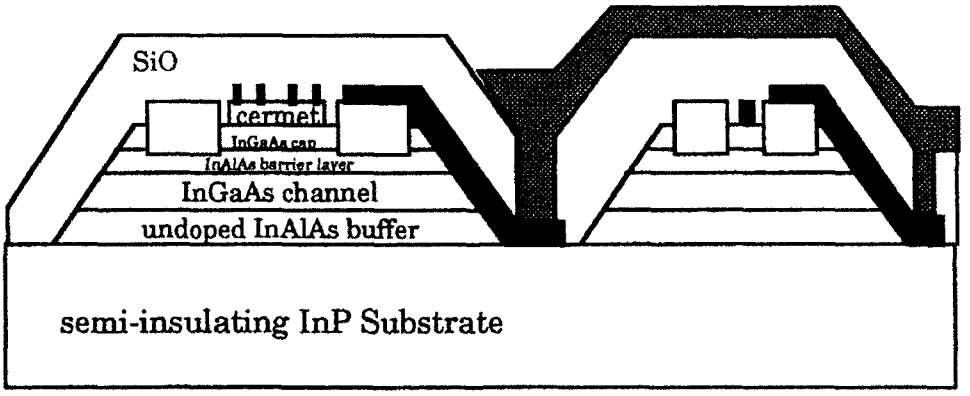


Figure 11: Interconnect metallization

Following processing, die containing 6 CCDs and one test structure were mounted in DIP packages for testing (Figure 12). A packaged device has been submitted along with this Final Report.

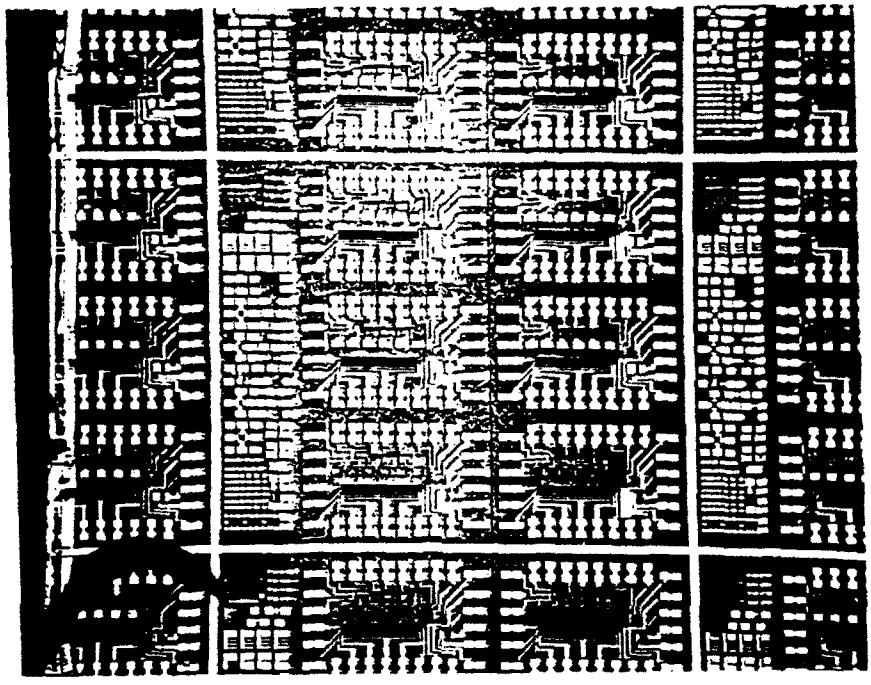


Figure 12: Processed CCDs and test structures

3.4 Characterize test structures and CCDs

The objective of Phase I of this Program was to demonstrate room temperature InGaAs CCD operation at frequencies applicable for readout of two-dimensional focal plane arrays. This development would serve as the foundation for Phase II, in which the InGaAs CCD would be used separately as a direct detection two-dimensional focal plane array, and as a readout for two-dimensional photodetector arrays, thus realizing a monolithic InGaAs focal plane array for near infrared detection.

Phase I was partially successful in that the characterization of various test structures indicated that the majority of the device fabrication steps were successful and resulted in functional device elements which make up the CCD, concomitantly indicating that the target material parameters were achieved. Full CCD operation was not achieved due primarily to a failure in one step of the fabrication process. Specifically, the second metallization level suffered from poor step coverage of the via to the first metal layer, thus precluding testing of the CCD delay lines.

3.4.1 Step Coverage

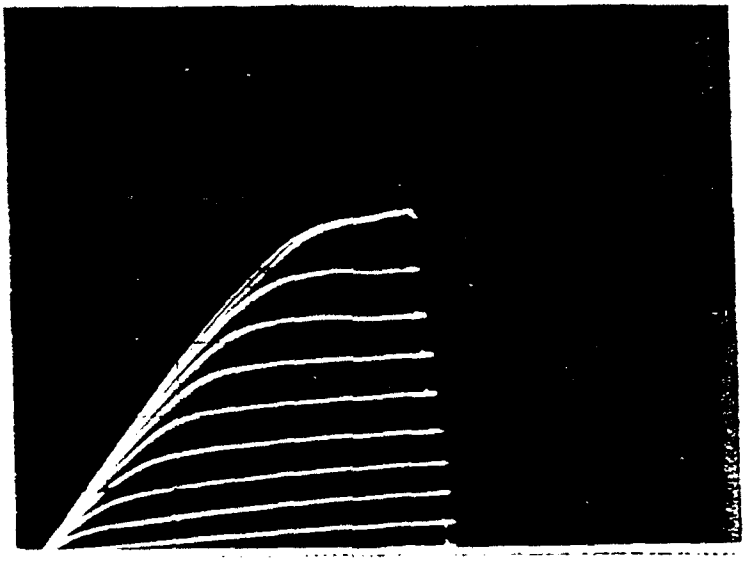
Poor step coverage proved to be the essential problem which prevented demonstrating CCD performance. Each chip includes two via chain test sites (i.e., each via chain contains greater than 80 series connected vias) which are typically used for estimating the via contact resistance. Each of the twenty-four via chains tested on twelve chips was open circuited. Of course, measuring an open circuit on these test structures only requires one open circuited via connection.

The extent of this problem was exemplified during probing of the CCD delay lines for preliminary characterization. Each of the twenty-four bonding pads to a delay line is formed from the second metallization on the substrate and must step cover the interlayer dielectric. For all bonding pads except the connections to the phases, the bonding pad metallization layer resting on the interlayer dielectric accesses the first metallization connection through four parallel via connections near the bonding pad location. Each of the phase bonding pads connects gate electrodes of the same phase through 33 parallel via connections near the delay line. While characterizing the CCDs, nearly all of the several hundred bonding pads that were probed were found to be open circuited at their respective junctures where the second metal layer was required to step cover the interlayer dielectric. The location was determined by placing a probe on the metal to either side of the step. It was also found that the open cir-

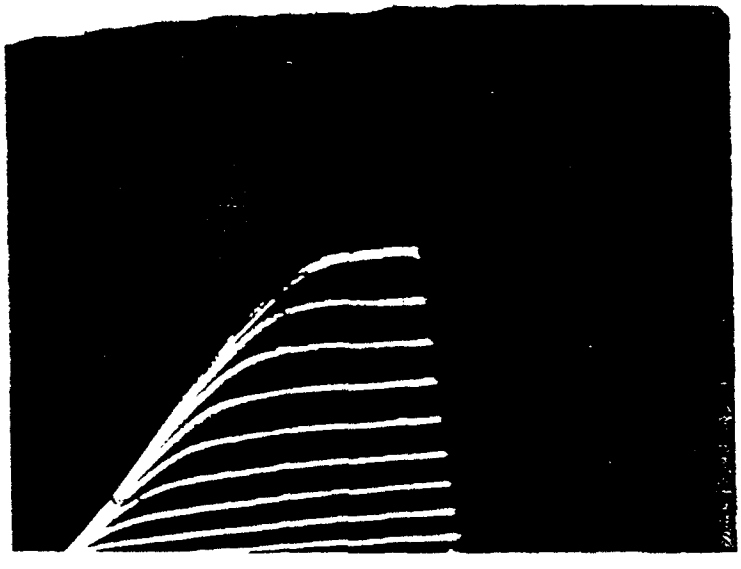
cuit could be closed by "dragging" a probe across the step and within the via, indicating that the cause of the open circuit vias is due to metal step coverage as opposed to, for example, incomplete etching of the vias. Since each of the four phases of the CCD contains 33 via connections, in view of the apparently widespread via connection failure, the delay line performance could not be tested.

3.4.2 MESFET Characteristics

Figures 13a and 13b illustrate the characteristics for MESFETs having a conventional metal gate (i.e., TiPtAu) and a cermet gate, respectively. The transconductance is estimated a 70 mS/mm, while the threshold voltage is about -4.5 V which corresponds to the expected value based on the designed device structure, thus indicating that the material growth achieved the target doping levels and thicknesses. In addition, these characteristics indicate good FET breakdown characteristics; the FETs can sustain a drain-source voltage of at least 5 V with the threshold voltage applied to the gate. More importantly, operation of the resistive-gate FET is evidence that the resistive-gate structure modulates the channel potential, suggesting that the CCD channel gate structure should function properly in response to applied clocking signals.



(a)



(b)

Figure 13: Transistor characteristics for (a) a TiPtAu gate MESFET and (b) a cermet resistive-gate MESFET. Gate length = 2 μm; gate width = 100 μm; 5 mA/div; 1 V/div; -0.5 V/step.

3.4.3 Gate Leakage Current Characteristics

The leakage current for the CCD channel was characterized in order to estimate the limitations on performance. Excessive leakage current was measured and attributed to the leakage current component from the mesa sidewall, which is schematically depicted in Figure 14. Although this leakage source was expected, it far exceeded expectations. The sidewall leakage can be eliminated by further developing the fabrication process.

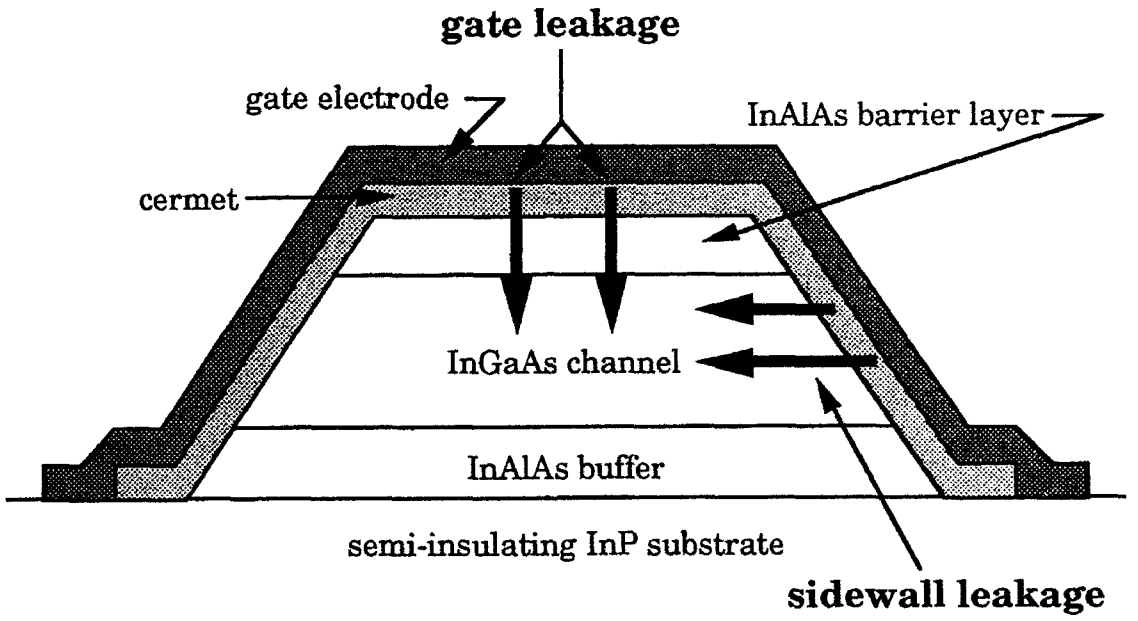


Figure 14: Schematic illustration of the leakage current components for the CCD mesa etched structure

Figure 15 shows the CCD channel leakage current measured for several delay lines at room temperature, and corresponds to a leakage current density of about 0.5 A/cm^2. This excessive leakage current is the second limitation on these devices. This large leakage current would require that the devices be tested at very high frequencies and/or low temperatures. As discussed above, however, the via interconnection failure precluded testing the delay lines.

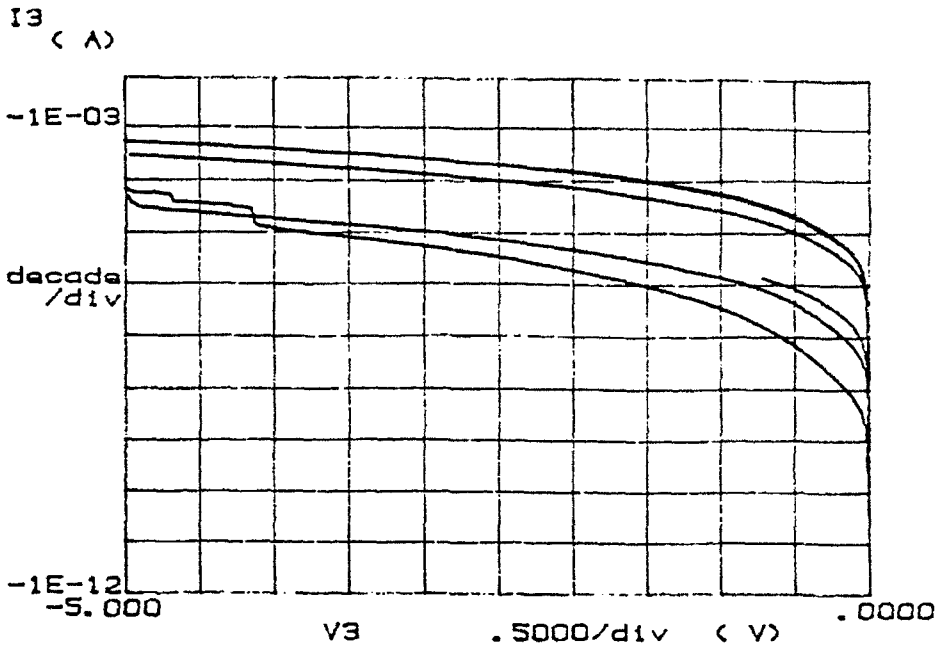


Figure 15: Room temperature CCD channel leakage current for several delay lines. Area = 2.5×10^{-4} cm^2

In order to ascertain the source of this leakage current, a test structure was measured which includes a diode with the cermet gate entirely confined on the mesa, and a diode of the same area with the cermet gate overlapping the sidewall of the mesa. A comparison of the reverse leakage current for these two structures is shown in Figure 16, which indicates that the "on-mesa" diode structure exhibits a gate leakage about four orders of magnitude smaller than the "over-mesa" diode. At -2.5 V reverse bias, the leakage current density is about 100 $\mu A/cm^2$ for the "on-mesa" diode. The large difference between the "on-mesa" and "over-mesa" diode leakage currents indicates that the predominant source of leakage current for the CCD structures is due to current flowing into the channel from the sidewall of the mesa where the cermet directly contacts the InGaAs channel (see Figure 14). Also note, that the leakage current for the "over-mesa" diode is of the same magnitude as the CCD channel leakage current (Figure 15).

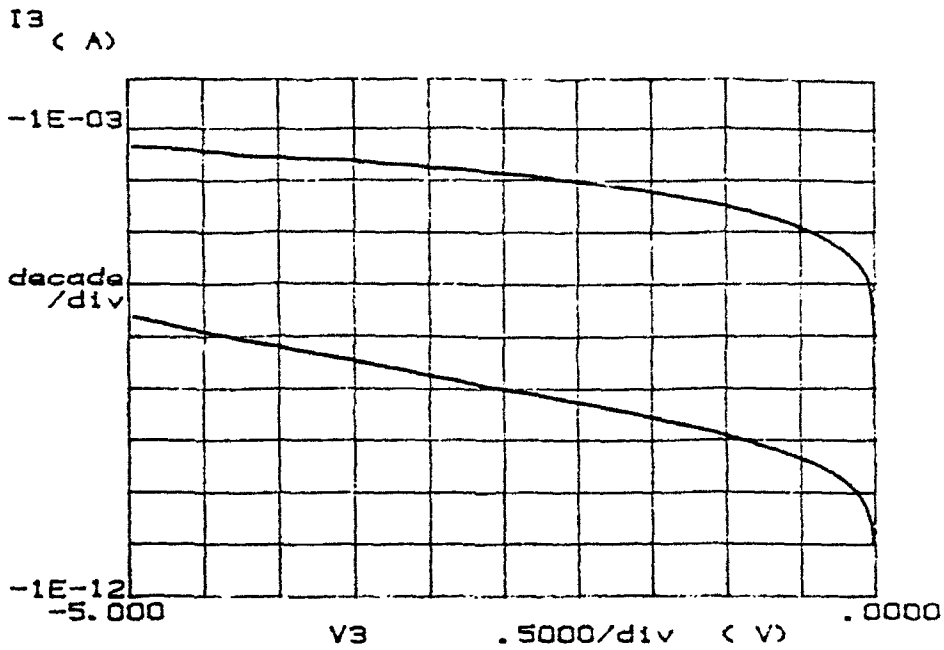


Figure 16: Room temperature leakage current for "on-mesa" diode (lower trace) and "over-mesa" diode. Area = 10^{-4} cm^2

This source of leakage was anticipated in the proposal stage of this project; however, due to constraints on the development of fabrication techniques outside the scope of those available at the fabrication location, and previous experience indicating that CCD performance could still be measured, steps were not taken to avert this problem. The magnitude of this leakage component exceeds that anticipated based on previous experience.

The unanticipated magnitude of the leakage current may partially be explained by the characteristics of the cermet layer. Cermet contacts have been shown to exhibit lower leakage current than conventional metallization, as illustrated in Figure 17 which compares a cermet diode and TiPtAu diode of equal areas. It is this attribute which suggested that the sidewall leakage would not necessarily have to be eliminated in Phase I in order to demonstrate CCD performance. Notably, previous devices have exhibited larger reductions in leakage current for cermet as opposed to conventional metallization than that exhibited in Figure 17.

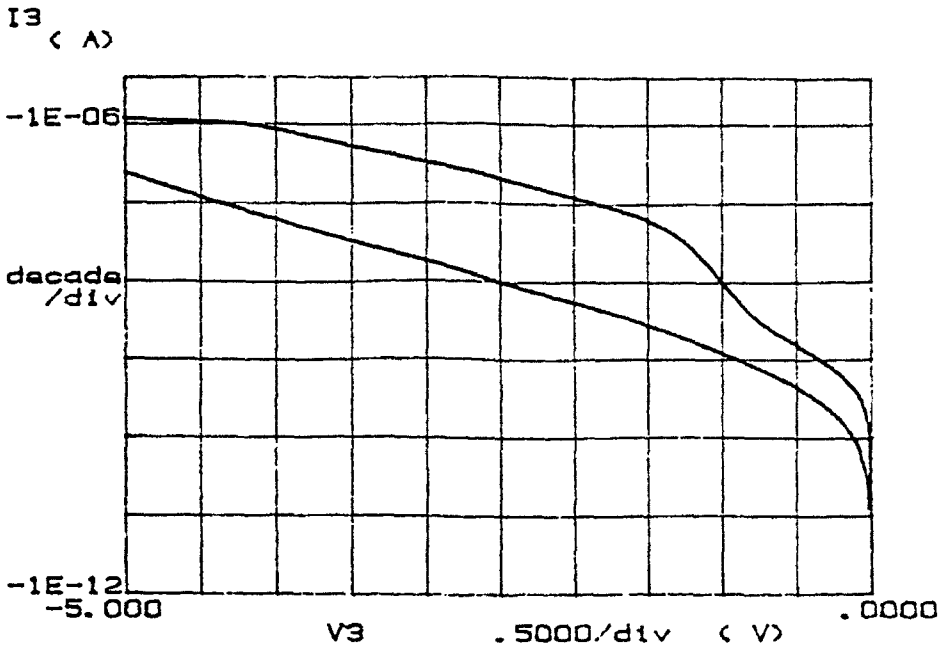


Figure 17: Room temperature leakage current for "on-mesa" diodes with a cermet contact (lower trace) and a TiPtAu contact

The maximum sheet resistance measured for the cermet layer was 130 KΩ/square (this measurement did not extract the contact resistance of the gate fingers which contacted the cermet during the measurement). Previous devices, however, employed sheet resistances two to three times this value. Since increasing the sheet resistance of cermet layers decreases the measured leakage current, the relatively low sheet resistance may be a factor contributing to the larger than expected sidewall leakage.

4.0 Conclusions and Discussion

CCD performance was not demonstrated in Phase I of this Program. Device characterization indicated that the exclusive problem was due to an avoidable fabrication error. Measurement of leakage current indicated excessive sidewall leakage current. Both of these problems may be overcome with further process development. In addition, the intrinsic leakage current suggests that room temperature operation for readout structures is possible.

Nevertheless, it is likely that the CCD would not be the device of choice in implementing a monolithic InGaAs focal plane array because of the stringent requirement for high quality, uniform material properties over large areas. Simply stated, because of the inherent shift register nature of CCDs, a single defective pixel will adversely affect the signal characteristics of all "upstream" pixels. In contrast, pixel defects in a multiplexed readout structure may be selectively compensated. Of course, characterizing CCDs fabricated on InGaAs is not only the ultimate test of the performance that can be achieved relative to other approaches, but also is a good measure of the material quality based on the yields these devices. In balance, by analogy to the commercial success of silicon CCDs, as material quality improves the CCD may become the natural choice for InGaAs imagers.

5.0 Phase II Activities

The overall conclusions from this and the related programs described in the Project Summary are:

1. In the near term, the hybrid approach of integrating an InGaAs photodiode array with a silicon readout multiplexer has the greatest chance of success with state-of-the-art room temperature imaging having been achieved in the 1-1.7 μm band. To extend this result to 1-3 μm will require substantial advances in both materials and processing technology.

2. As a follow-on technology, the monolithic focal plane array approach is realistic. A Phase II program is currently underway with a goal of demonstrating two dimensional imaging in the 1-1.7 μm band.

3. In the foreseeable future, CCDs are not a viable approach to NIR imaging in the InGaAs system. The reasons for this conclusion are discussed in this report. We do conclude, that the performance of linear CCDs is an excellent way to quantify advances in both materials and process technology.

Based on the above conclusions, a Phase II proposal will be submitted with a goal of using CCDs as a key element in a materials and process development program leading to monolithic, room temperature 1-3 μm imaging.